International Journal of Research in Advent Technology, Vol.2, No.4, April 2014

E-ISSN: 2321-9637

A Review of ECG Monitoring System Using Wavelet Transform

Bhushan N. Patil[1],
M.E. (Digital Electronics),
S.S.B.T's COET, Bambhori, Jalgaon, Maharashtra
Email: mr.bhushan5890@gmail.com[1]

Abstract- Day by day the scope & use of the electronics concepts in bio-medical field is going to increase step by step. Here in this paper the study of newly developed concepts is done for the monitoring of the ECG signal The paper just reviews & describes a power and area efficient electrocardiogram (ECG) acquisition and signal processing application sensor node for wireless body area networks (WBAN). This sensor node can accurately record and detect the QRS peaks of ECG waveform with high-frequency noise suppression. The metal–oxide–semiconductor technology with two chips: analog front end integrated circuit (IC) and digital application specific integrated circuit (ASIC) , where the analog IC consumes 79.6 µW and digital ASIC consumes 9 µW at 32 kHz with 1.2 mm^2. So, this ECG sensor node is convenient for long-term monitoring of cardiovascular condition of patients, and is very suitable for WBAN applications. The novelty of the design is that the introduction of reconfigurability to the analog front-end system so that it can extend to handle different kinds of bio-potential signals by just using the same analog IC chip.

Index Terms- Application specific integrated circuit, Electro-Cardio-Gram , Wireless Body Area Network , analog front end**.**

1. INTRODUCTION

1.1 Necessity

For the purpose of ECG monitoring, various types of QRS peak detection algorithms methods including filter-banks method [5], artificial neural networks, genetic algorithms, and geometrical matching approach are used. Most of such algorithms have comparatively high computational complexity and are not very suitable to be implemented in application specific integrated circuits (ASICs). The variety of QRS complex shape morphologies causes the performance of QRS complex detection algorithms that use fixed bandwidth band-pass filters and fixed width integration windows to decrease when the QRS morphology changes. To avoid this problem, a new approach to QRS complex detection based on wavelet transform (WT) is to be used.

1.2 Objectives

To study & review a ECG monitoring signal possessing system which can overcome following challenges:

ECG is considered to be a weak signal. According to [1], the signal amplitude can range from 100µV to 4 mV.

The main bandwidth of ECG signals spans from 0.1 to 250 Hz, whereby flicker noise is dominant.

This signal is susceptible to common-mode interference from the mains supply

The problem of offset generated by skin–electrode interface.

With this kind of condition, the analog front-end should be able to provide enough noise rejection in order to be able to amplify such signal. The gain and bandwidth of the front-end amplifier should be adjustable in order to deal with the different characteristic of the signal.[14]

1.3 Theme:

The basic theme of this paper is to study & review a new approach of DWT for ECG monitoring & acquisition ASIC system for WBAN. The metal–oxide–semiconductor technology with two chips: analog front end integrated circuit (IC) and digital application specific integrated circuit (ASIC) , where the analog IC consumes only 79.6 µW and digital ASIC consumes 9 µW at 32 kHz. Therefore, this ECG sensor node is convenient for long-term monitoring of cardiovascular condition of patients, and is very suitable for WBAN applications.

1.4 History

When we look out history For the purpose of ECG monitoring, various types of QRS peak detection algorithms methods including filter-banks method [5], artificial neural networks , genetic algorithms, and geometrical matching approach are used until now. Most of such algorithms have comparatively high computational complexity and are not very suitable to be implemented in application specific integrated circuits. The variety of QRS complex shape morphologies and causes the performance of QRS complex detection algorithms that use fixed bandwidth band-pass filters and fixed width integration windows to decrease when the QRS morphology changes. To avoid the problem, a new

approach to QRS complex detection based on wavelet) should be used [14].

Orgnization Of The Paper:

This paper is organized in five parts. First part is introduction. It gives the basic idea about ASICs & wireless Body Area Network. It explains the theme , objective , necessity & organization of the paper topic also it tells about literature serve. It also gives the history of the paper. It gives the different approaches which had been used until now.

Second part describes detail operation of the system. Also all the mathematical analysis is provided here. All the algorithm are also attached here which explains system operation.

Third part is about architecture of the system. This part also gives detail design methodology of the system. Information about every circuit element is given.

Fourth part is about Results of the system.The discussion about the cases is provided here to clear the concept.

Finally in the last part conclusion is provided which describes how the DWT approach is more efficient than other approaches. Also the scope of the system for future is discussed. At the last acknowledgement & the list of the references used is given.

2. METHODS USED & OPERATION

2.1 Discrete Wavelet Decomposition

Def- " The wavelet transform is a tool that cuts up data, functions or operators into different frequency components, & then studies each component with a resolution matched to its scale "

The digitalized ECG waveform from decimator filter is fed into the digital ECG signal processing module. For ECG monitoring purpose, the QRS peaks of ECG need to be detected. The received ECG signal is normally corrupted by many types of interference, like circuit noise and other biomedical signals. If we directly detect the QRS peak using the original recorded waveforms, it may downgrade the detection performance due to noise. .In order to effectively enhance the QRS feature extraction stage including

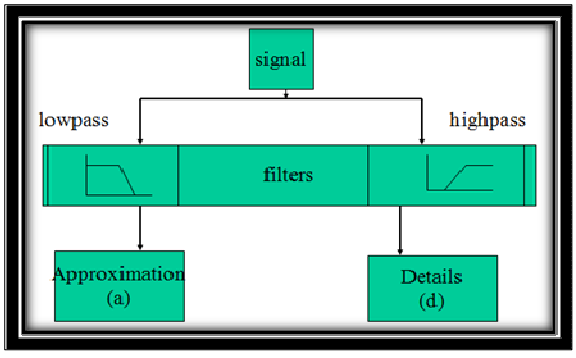


Fig. 1 Analysis of DWT

linear or nonlinear filtering and a decision stage decomposition LPF S_{2j} f(n) and decomposition HPF including peak detection and decision logic. Therefore, to avoid the issues of time-shifting and resolution degradation, we apply the same sampling rate in all scales. For scale , the outputs of

W_{2j} f(n) are given by [14].

S_{2j} f(n) = $\sum h^j_k . S_{2j-1}$ f(n-k) ……Eq.(1)

W_{2j} f(n) = $\sum g^j_k . S_{2j-1}$ f(n-k) .....……Eq.(2)

Here, h^j_k - is the coefficients of LPF

g^j_k - is the HPF of scale j.

2.2 Threshold Based Noise Suppression

The multi-scale analysis of wavelet transform can characterize ECG signals very well. Therefore, we first use the multi-scale information of WT to suppress the noise and then detect the QRS peaks. To exploit the wavelet inter-scale dependencies, multiply the adjacent outputs of decomposition HPF to enhance the edge structures while weaken noise. Following that, a threshold is calculated and imposed on the products, to find the important features.

The high frequency noise suppression algorithm based on multi-scale WT is depicted in Fig- 2 Suppose the noise yields small-value wavelet coefficients while the large coefficients are composed mostly of the useful signal. By taking the advantages of the dependency information between wavelet scales, the high pass filter outputs of two adjacent scales are multiplied to amplify the significant features and dilute noise. The procedure of the proposed de-noising algorithm is as : [14].

Compute the multi-scale product

$$P_j f(n) = W_2^j f(n).W_2^{j+1}, \quad for \quad j=2,3$$

… …….Eq.(3)

Preset the thresholds t_j by calculating the standard deviation of P_j f(n) for each window with a specified number of samples

$$t_j = \epsilon_j [P_j f(n)] , \quad j = 2 , 3$$

… …….Eq.(4)

Denoise HPFs W_{2j} f(n) based on the threshold t_j

$$W_{2j} f(n) = \begin{cases} W2j\ f(n), & |P_j f(n)| \geq t_j \\ 0, & |P_j f(n)| \leq t_j \end{cases}$$

for j =2 , 3 . ..……Eq.(5)

2.3 Threshold Based Noise Suppression

The high frequency noise suppression algorithm based on multi-scale WT is depicted Fig- 3 Suppose the noise yields small-value wavelet coefficients while

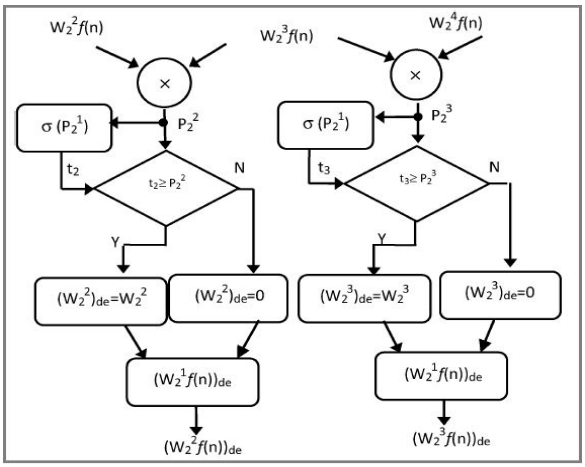


Fig. 2 Block diagram of the de-noising algorithm [14]

the large coefficients are composed mostly of the important signal. By using the dependency information between wavelet scales, the HPF outputs of two adjacent scales are multiplied to amplify the significant features and dilute noise. The procedure of the de-noising algorithm is summarized as follows [14]

problem because it has a time-varying morphology and is subject to physiological variations due to the signals, readers are referred. Because the QRS complexes have a time-varying morphology, they patient and noise corruption. For a tutorial on ECG are not always the strongest signal component in an ECG waveform. So, P-waves or T-waves with characteristics matches to that of the QRS complex, as well as spikes from high frequency pacemakers compromise the detection of the QRS complex [11]. There are many sources of noise in a clinical environment that can degrade the signal. Including power line interference, poor electrode contact with body, patient movement & baseline wandering. So, QRS detectors must be invariant to different noise sources should be able to detect complexes even when the morphology of the ECG signal is changing with

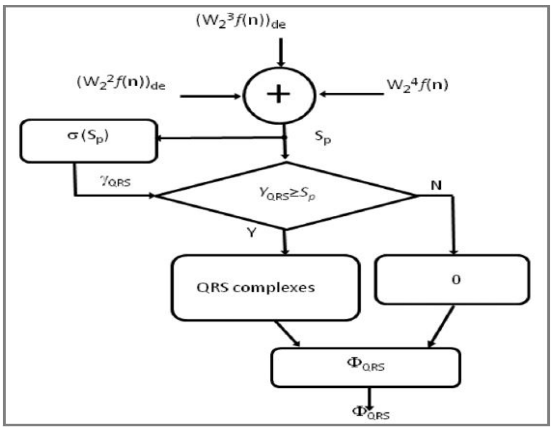


Fig. 3 Block diagram of the QRS detection algorithm.[14]

time [11]. After the noise components of high pass filter outputs in scales 2-3 suppressed, the HPF output of scale 4 & the de-noised HPF outputs of scales 2-3 are added point-by-point to increase the QRS complex while suppress the noise [14].

The summation is defined as :

$$S_P(n) = \{W_2^2 f(n)\}_{de} + \{W_2^3 f(n)\}_{de} + \{W_2^4 f(n)\}_{de}$$

. . ……Eq.(6)

Finally, to perform the decision-making for detecting QRS complexes an adaptive thresholding scheme is applied to the feature waveform generated from the summation stage. The thresholding scheme can be formulated as :

$$\#(QRS) = \begin{cases} 0, & Sp(n) < \gamma QRS \\ 1, & Sp(n) \geq \gamma QRS \end{cases}$$

……Eq.(7)

Where, $\#(QRS)$ locates the position of QRS complexes and denotes the adaptive threshold. The adaptive threshold in the decision rule is updated by :

$$\gamma QRS = c.\sigma.\{Sp(n)\} \; . \qquad \text{.....Eq.(8)}$$

Thus from above equation the QRS complexes can be detected using thresholding..

3. SYSTEM ARCHITECTURE

3.1 System Demonstration

Fig- 4 represents demonstration of digital ECG signal processing application specific integrated circuits, which achieves low power consumption & high hardware efficiency. This paper only focuses on the digital system architecture and circuitry design. In this review paper, we study a reconfigurable analog front-end and ADC, which interfaces with the DSP module, so that a ECG acquisition and monitoring system is demonstrated for WBAN applications with ultra-low power and small si area.[14]

3.2 Genaral Architecture

Architecture of Front end & Back end of the system :

Since the front-end is a reconfigurable design which can be applicable for other biomedical applications

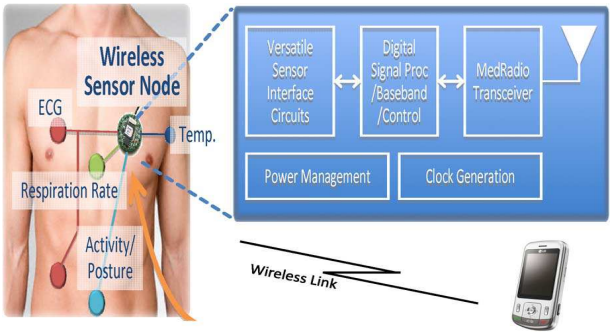


Fig. 4 Demonstration of WBAN technique.[14]

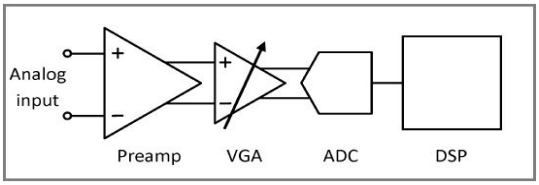


Fig. 5 Front end ECG monitoring system Architecture

.

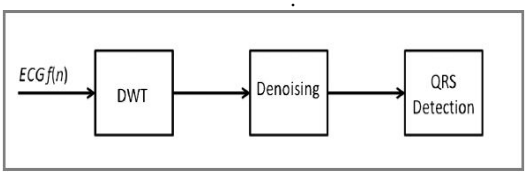


Fig. 6 Back End Digital signal processing ASIC for ECG.

also, a two-chip solution is studied. In the signal acquisition ASIC, the gain & bandwidth of the front-end are adjustable & a low power sigma-delta ADC is used. In the digital ECG signal processing ASIC, the real-time accurate QRS peak detection is based on WT with high frequency noise suppression. To acquire the ECG waveform and digitalization, design includes integrated analog ECG acquisition front-end, with a chopper- stabilized preamplifier, a variable gain amplifier & a 3rd-order sigma-delta ADC with digital decimation filter. In the digital ECG signal processing application specific IC, to exploit the wavelet inter-scale dependencies, multiply the adjacent wavelet sub- bands for enhancing the edge structures while weakening noise. So, a threshold is calculated and imposed on the summation to identify the important features. So, design achieves low error rate peak detection. The chip enables the signal processing at the sensor node with low area and power consumption. Combined with wireless transceiver, the ECG QRS information can be extracted & wirelessly transmitted to the healthcare server for monitoring & diagnosis purpose. So, this ECG ASIC is very suitable for battery-supplied healthcare WBAN applications.[14]

3.3 Architecture of a complete WBAN radio transceiver

Following that, the received PSDU is fed into the MAC layer as shown. To achieve ultra low power Fig.

Working environment	Indoor WBAN application
Working range	1~5m
Required raw data rate	250kbps
Required SNR for 1 %	17dB
Target power consumption	<100µW

Table. 1 System Requirement of the System [13]

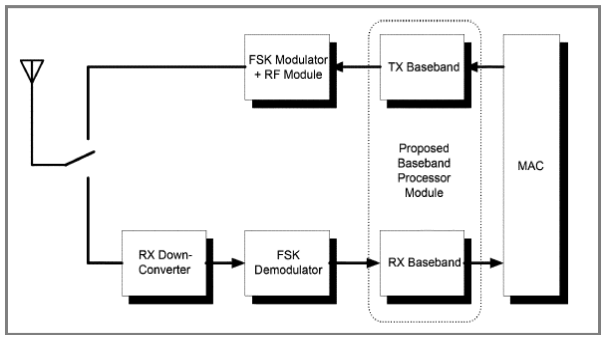


Fig. 7 Block diagram of a complete WBAN radio transceiver.[13]

consumption of power, a low PHY specification is used. The signal processing flow for TX & RX are presented in Fig -8 & 9. The baseband processor constructs the PPDU, it's structure is illustrated in The permitted length of the PSDU within one packet should be less than 127 octets & this contained in the PHY header in octets. Once one packet of the PSDU is generated using MAC layer, The complete system diagram of a WBAN radio transceiver is shown in Fig. In the TX block, the physical layer service data unit from the MAC layer is in the transmitter baseband processor module to generate a physical layer protocol data unit packet. The channel coding & signal processing are performed on the PPDU in the TX baseband processor module & the raw data rate of the TX baseband processor module output is 250 kb/s. The baseband raw data is modulated by frequency shift keying & directly up-converted to a 2.45 GHz radio frequency signal. In the receiver (RX) block, the received RF signal is down-converted to intermediate frequency signal & demodulated by a low power FSK demodulator. it is given to TXFIFO & ready to transmission. There is a Prefix MUX block controlled by the TX state control block which selects input of the Hamming encoder.

AS a transmission command is sent from the MAC layer, the PHR is prefixed to the PSDU & sent into the Hamming encoder block . The input data of the Hamming encoder is in sequence with 1 bit word length. IHamming coding and 8,4 matrix interleaving are used as forward error correction coding. For each consecutive 4 bits of input, the Hamming encoder generates 8 bits of output and so the word-length of the Hamming encoder block output is 8 bits. [13]

The output data of the Hamming encoder block is fed into the 8,4 matrix interleaving block for suppressing the burst error. To eliminate long strings of like bits that impair receiver synchronization & for eliminating most periodic bit patterns that produces undesirable frequency components, the interleaved data payload is fed to a scrambling block & it is coded by a Manchester encoder. It generates the scrambling code in sequence with 1 bit word-lengthThe output data of it is in serial sequence with 1 bit word-length & is XORed with the generated code. The scrambled data

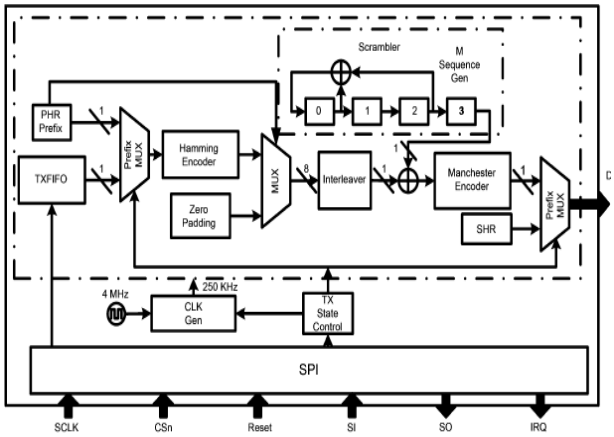


Fig. 8 Block diagram of baseband Transmitter. [13]

payload is fed to the Manchester encoder. The Manchester encoder changes the bit "0" to bits "01" & changes the bit "1" to bits "10," thus the total number of "0" & "1" can be balanced. The output of the Manchester encoder is prefixed with the synchronization header & is sent to the FSK modulator for transmission. The D flip-flop provided by the technology library to sample & to restore the input. If input signal is higher than of the D FF, the output of the D flip-flop will be "1." If input signal is lower than of the D flip-flop, the output of the D FF will be "0." The received data stream is the demodulated binary signals from the frequency shift keying demodulator. As shown in Fig, the signals are first fed into the synchronization and data recovery block to achieve synchronization & to recover the data. The SDR over-samples the incoming signal using a shift register matrix & calculates the

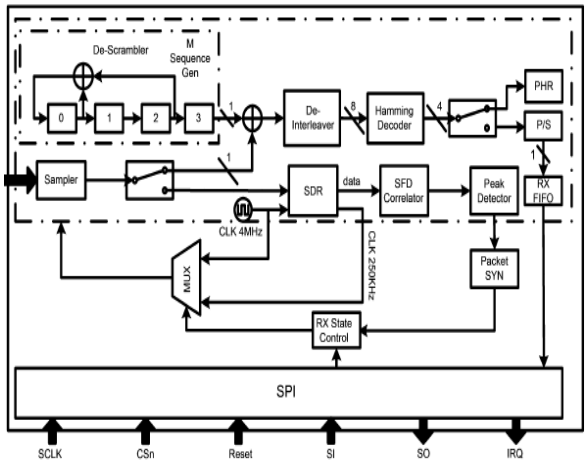


Fig- 9 Block diagram of baseband Receiver. [13]

		Octets		
		1		1 ~ 127
Preamble	SFD	Reserved (1 bit)	Packet length (7 bits)	PSDU
SHR		PHR		PHY payload

Fig- 10 PPDU packet format. [13]

correlation between the incoming data and the predefined preamble sequence. The peak of the calculated correlation is detected continuously. [13]

Once the peak value is found, the start-of-frame delimiter Co-relater calculates the correlations between the incoming data & the predefined SFD sequence & the peak value is searched.

Once the peak value is found, the packet synchronization is done. The preamble sequence and SFD are removed & the Packet SYN block indicates the RX State Control that the PHR & PSDU received. The SDR block also creates the 250 kHz clock & the RX State Control block selects the operation clock frequency for baseband processor module which is between 4 MHz & 250 kHz clock. Manchester decoding is performed on the received PHR and PSDU data sequentially.[13]

4. CIRCUIT DESIGN

4.1 Chopper-Stabilized Preamplifier :

The preamplifier is mainly used to provide a necessary amplification to the signal without introducing significant noise from the devices. For this reason, chopper stabilization was selected to primarily remove the noise that might deteriorate the SNR at the intended low frequency application. Fig-11 shows the circuit schematic of the preamplifier. The preamplifier was designed based on negative feedback gm-boosted source degenerated differential pair with resistive loads. The topology in was modified by a CMFB to generate the desired common mode voltage at the amplifier output. The resistive load was replaced with MOS load transistor. The loading effect to set the respective gain is performed by placing a resistor with each node connected to each output of the amplifier. Chopper stabilization is employed by placing a modulator before the input and a demodulator after the output of the amplifier. A 4^{th} order LPF follows the amplifier to remove noise & dc offset of the amplifier The 4^{th} order LPF off frequency of 2.57 KHz, the 4^{th} order filter is sufficient to provide attenuation of 60 dB. A ring oscillator was used to provide an on-chip 16 kHz chopper signal.

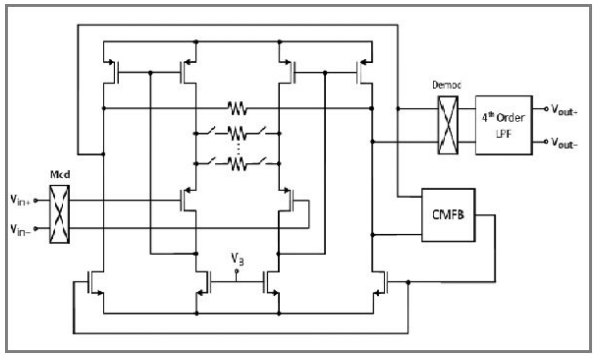


Fig- 11 Circuit schematic of chopper-stabilized preamplifier.[14]

pair of capacitors is used before pre-amplifier to remove dc offset, to facilitate the fast prototype of the system. The CMRR of the overall system is so limited because of the non-perfect matching of capacitors. The power-noise efficient preamplifier design by Yazicioglu is potentially be incorporated into future design of the system.

4.2 Variable Gain Amplifier :

It is used to amplify the signal, while providing flexibility in setting the amplification factor & pass-band BW. Fig- 12 shows the system structure of the VGA. It has 3-bit gain control & 4-bit BW control. Structure of the VGA can be divided into 2 stages. The 1st stage is an OTA with source degenerated differential pair. It performs gain control by tuning the value of source degeneration resistor. The 2nd stage is a pass-band block that provides tuning of the gain and control of the bandwidth. This stage comprises of gain-BW control block, followed by an OTA. The gain tuning is done through gain-BW control block by changing the value of capacitor on its output. This capacitor, together with capacitor, forms capacitive divider. The bandwidth control is done by tuning the value of capacitor at the input of this block.
This capacitor acts as a load for the OTA on the first stage. The VGA was designed to have gain range from 8 to 58 dB. The high-pass corner was set at 0.015 Hz and the low-pass corner is tuneable from 100 Hz to 2 kHz. [14]

4.3 Sigma–Delta ADC :

The analog-to-digital (A/D) interface system proposed in this paper will be suitable for battery-powered (portable) medical equipment such as, electro-oculogram, electroencephalogram , electrocardiogram , electro-myogram (EMG), and axon action potential (AAP). There are several commercial products in the world market of medical devices for ECG measurements and, some of them are even portable. However, all of these systems are only oriented for ECG applications and, therefore, they are not suitable for EOG, EEG, EMG, or AAP measurements. [9] On the other hand, these systems are supplied with several batteries of 1.5 V and dissipate a considerable amount of power. Both low-voltage operation and low-power dissipation are of great importance for portable applications Low-voltage operation is demanded because it is needed to use as few batteries as possible for size & wt. considerations. Low current consumption is needed for ensuring a reasonable battery lifetime. These data-acquisition systems comprise typically a low-noise PGA followed by an anti-aliasing & by a Nyquist-rate analog to digital converter. It introduces several performance limitations like the signal bandwidth is determined by the cut-off frequency of the AAF. The resolution of the ADC is around 10–12 bits there is no dynamic range to deal with a strong signal & with very small signals pretended to be measured filter to have a bandwidth of 500 Hz [9]

Sigma–delta modulator is employed together with digital decimation filter. Single-loop 1-bit sigma-delta ADC was selected as its simplicity and insensitivity imperfections of analog circuits. System level simulations in MATLAB can be performe in order to derive the modulator requirements and specifications for individual sub-blocks. In most of ECG/EEG acquisition applications, the requirement of ENOB of analog to digital is at least 8 bits. It can be found that 3rd order meets this requirements & with good signal shaping capacity. Fully-differential current mirror OTA is used to accommodate the low supply voltage & to provide more power efficiency for the system. Bootstrapped switch reported in is adopted. Switch was designed to operate at low voltage with device reliability. The single bit quantizer is realized with a high dynamic comparator with an SR latch. The comparator is a dynamic circuit & it consumes a very low power . The switching clock is derived as an on chip clock generator to give choice on over sampling ratio of 32. Following the ADC, a decimation filter is used as shown in Fig. 14.

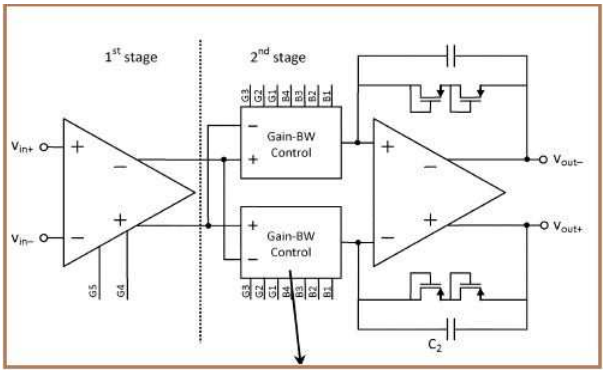


Fig. 12 System structure of VGA.[14]

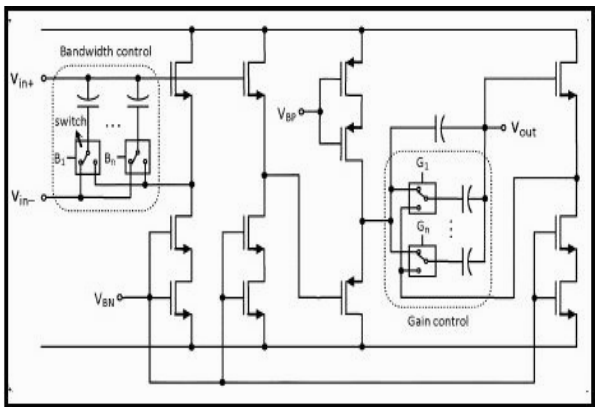


Fig. 13 System structure of VGA.

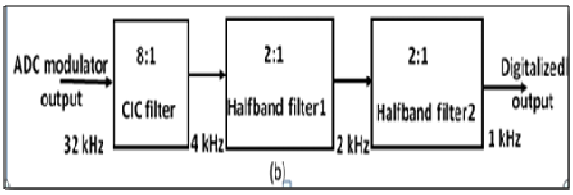
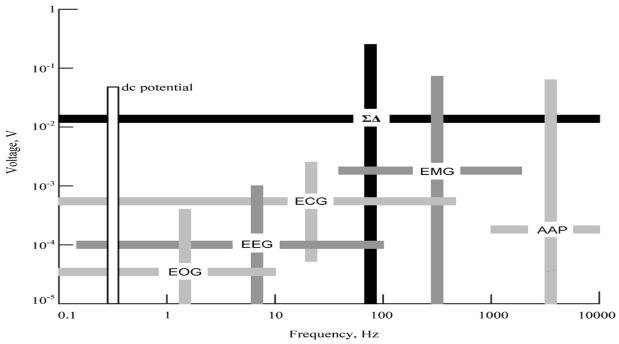


Fig. 14 Block diagram of decimation filter[14]



Graph. 1 Voltages & frequency ranges of some common bio-potential signals [9]

Gray color -Voltages and frequency ranges of some common bio-potential signals
White color -DC potentials include intracellular voltages as well as voltages measured from several points on the body
Black-color -The required DR and BW

The filter consists of one cascaded integrator-comb filter & 2 stages of half-band filters. The decimation filter is used to reduce the sampling rate of ADC output and to suppress the out-of-band noise.[13]

The main advantages of this architecture are as follows :
1) It is flexible, as it is suitable for digitizing several bio-potential signals.
2) It is designed for low-voltage and low-power operation using a mixed CB/SO approach i.e., suitable for portable equipment.
3) The required Galvanic isolation can be performed in the digital domain using an opto-coupler.

CONCLUSION

A real-time on-chip ECG signal processing system is designed. The proposed design includes an analog ECG acquisition front-end and a digital QRS peak detection module. The QRS peak detection scheme is based on the four-scale wavelet transform algorithm, and can achieve accurate QRS peak detection performance using multi-scale wavelet based de-noising procedure. The proposed ECG signal processing system consumes ultra low power and small silicon area, and thus is extremely suitable for long-term cardiovascular monitoring WBAN applications.

REFERENCES

[1] Abo A. M. ; Gray P. R. (1999) : A 1.5-V, 10-bit, 14.3-MS/s CMOS pipeline analog-to-digital converter, IEEE J. Solid-State Circuits, vol. 34, no.5, pp. 599–606.

[2] Afonso V. X.; Topkins W. J.; Nguyen T. Q.; Luo S. (1999) : ECG detection using filter banks, IEEE Trans. Biomed. Eng., vol. 46, no. 2, pp. 192–202.

[3] Bonato P. (2003) : wearable sensors/systems and their impact on biomedical engineering, IEEE Eng. Med. Biol. , vol. 22, no. 3, pp. 18–20.

[4] Bonato P. (2011) : Multiple Functional ECG Signal Is Processing For Wearable Applications Of Long-term Cardiac Monitoring, IEEE Transactions On Biomedical Engineering, VOL. 58, No. 2.

[5] Borromeo S.; Rodriguez-Sanchez C.; Machado F (2007) : A reconfigurable, wearable, wireless ECG system, in Proc. IEEE 29th Annu. Int. Conf. Eng.Med. Biol. Soc. (EMBS), pp. 1659–1663.

[6] Bradie B. (1996) : Wavelet packet-based compression of single lead ECG,IEEE Trans. Biomed. Eng., vol. 43, pp. 493–501.

[11] Cohen A.; Kovaˇcevi´c J. (1996) : Wavelets: The mathematical background, Proc. IEEE, vol. 84, no. 4, pp. 514–522.

[8] Crouse M. S.; Nowak R. D.; araniuk R. G. (1998) : Wavelet-based statistical signal processing using Hidden Markov models, IEEE Trans. Signal Process., vol. 46, no. 4, pp. 886–902.

[9] Goes J. ; Paulino N. ; Pinto H. ; Monteiro R. (2005) : Low power low-voltage CMOS A/D sigma-delta modulator for biopotential signals driven by a single-phase scheme, IEEE Trans. Circuits Syst., vol. 52, no. 12, pp. 2595–2604.

[10] Guo D. G.; Tay F. E. H.; Yap K. L. (2008) : A Wearable BSN-based ECG-recording System Using Micromachined Electrode forContinuous Arrhythmia Monitoring, in Proc. IEEE 5th Int. Workshop Wearable Implantable Body Sens. Netw., pp. 41–44.

[11] Kadambe S.; Murray R.; Boudreaux-Bartels G. F. (1999) : Wavelet transform-based QRS complex detector, IEEE Trans. Biomed. Eng., vol. 46, no. 7, pp. 838–848.

[12] Li C.; Zhang C.; Tai C. (1995) Detection of ECG characteristic points using wavelet transforms, IEEE Trans. Biomed. Eng., vol. 42, no. 1, pp. 21–28.

[13] Liu X.; Zheng Y. J.; Zhao B.; Wang Y. S.; Phyu M. W. (2010) : An ultra low power baseband transceiver IC for wireless body area network in 0.18 µm CMOS technology, IEEE Trans. Very Large Scale (VLSI) Syst., vol. 19, no. 8, pp. 1418–1428.

[14] Liu Xin ; Zheng Yuanjin ; Myint Wai Phyu ; Endru F. N. ; Navaneethan V. (2012) : An Ultra-Low Power ECG Acquisition and Monitoring ASIC System for WBAN Applications IEEE Journal On Emerging And Selected Topics In Circuits And Systems, VOL. 2, NO. 1.

[15] Murray R. (1994) : Performance of DyWT QRS detector on the AHA database," Univ. Rhode Island, Kingston, RI, Tech. Rep. 0994-0001.

[16] Meste O.; Rix H.; Caminal P.; Thakor N. V. (1994) : Ventricular late potentials characterization in time-frequency domain by means of a wavelet transform," IEEE Trans. Biomed. Eng., vol. 41, pp. 625–634.

[17] Sadler B. M. ; Swami A. (1999) : Analysis of multiscale products for step detection and estimation, IEEE Trans. Inf. Theory, vol. 45, no. 3, pp. 1043–1051.

[18] Omeni O.; Wong A. C. W.; Burdett A. J.; Toumazou C. (2008) : Energy efficient medium access protocol for wireless medical body area sensor networks, IEEE Trans. Biomed. Circuits Syst., vol. 2, no. 4, pp. 251–259, Dec. 2008.

[19] Mercier P. P.; Chandrakasan A. P. (2010) : A 110 W 10 Mb/s eTextiles transceiver for body area networkswith remote battery power," in IEEE ISSCC Dig., pp. 496–497.

[20] N. V. Thakor, G. X. Rong, S. Y. Chun, and D. F. Hanley, "Multiresolution wavelet analysis of evoked potentials," IEEE Trans. Biomed. Eng.,
vol. 40, pp. 1085–1094, Nov. 1993.

[21] Papadimitriou S.; Gatzounas D.; Papadopoulos V. (1996) : Fetal heart rate signal denoising by processing the wavelet transform modulus maxima, in Proc. Annu. Int. Conf. IEEE EMBS,vol. 18.

[22] Sahambi J. S.; Tandon S.; Bhatt R. K. . (1997) : Using wavelet transform for ECG characterization, IEEE Eng. Med. Biol., vol. 16, no. 1, pp. 77–83.

[23] S. Mallat, (1992) : Characterization of signals from multiscale edges, IEEE Trans. Pattern Anal. Mach. Intell., vol. 14, no. 7, pp. 710–732.

[24] Teo T.; Gopalakrishnan P.; Pang C. Y. (2009) : A 700-µWsingle-chip IC for wireless continuoustime health monitoring in 0.18-µm CMOS, in Proc. IEEE Asian Solid-State Circuits Conf., 2009, pp. 361–364.

[25] Tuzman A.; Acosta M.; Bartesagh R (1996) : Wavelet-based compression of Holter ECG signals," in Proc. Annu. Int. Conf. IEEE EMBS, vol. 18.

[26] Wong A. C.; McDonagh D.; Kathiresan G.; O. Omeni C. (2008) : A1 V, micropower system-on-chip for vital-sign monitoring in wireless body sensor networks, in IEEE ISSCC Dig., pp. 138–139.

[27] Walker James S. (1997) : Fourier Analysis and Wavelet Analysis, Notices Of The Ams , Volume 44, Number 6.

[28] Ye D.; Ouyang X. (1996) : Application of wavelet analysis in detection of fetal ECG, in Proc. Annu. Int. Conf. IEEE EMBS, vol. 18.

[29] Zheng Y. ; Lin Z. (2003) : Recursive adaptive algorithms for fast and rapidly time varying systems, IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process., vol. 50, no. 9, pp. 602–614.

[30] Zou X. D. ; Xu X. Y. ; Yao L. B. ; Lian Y. (2009) : A 1 V 450 nW fully integrated programmable biomedical sensor interface system, IEEE J. Solid-State Circuits, vol. 44, no. 4, pp. 1067–1077.